



ASML

From High-Level Algorithms to ASML Automated Digital Design Flows

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Key Takeaways

1. ASML business drivers: Quality and Time-to-Market, require an efficient workflow for getting smart algorithms into high speed digital hardware (FPGAs)
2. Adoption of Model-Based Design into the ASML Digital Design Flow achieves this with automatic generation of HDL source code and test bench code
3. Model-Based Design reduces the gap between system architect and design engineer



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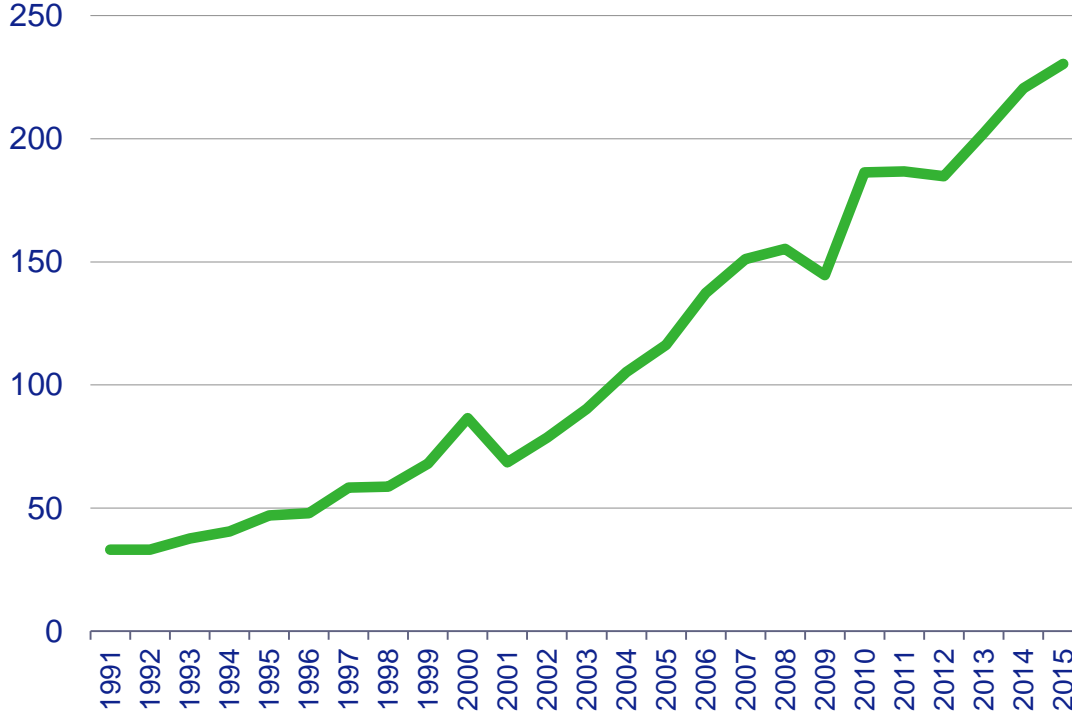
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WORK

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Chips are everywhere!

In 2015, 230 billion ICs were made, 30 for every man, woman and child on the planet

IC units, in billions



Semiconductor Revenue Milestones	
\$50B	1989
\$100B	1994
\$200B	2000
\$300B	2010
\$400B	2017
\$500B	2019

We develop and build lithography systems for manufacturing those IC's

150 tons of precision equipment



works with single nano-meter precision:
Grass grows at a speed of 33 nano-meter per second



Moore's Law means doing "More with Less"



Cray Super Computer
1976

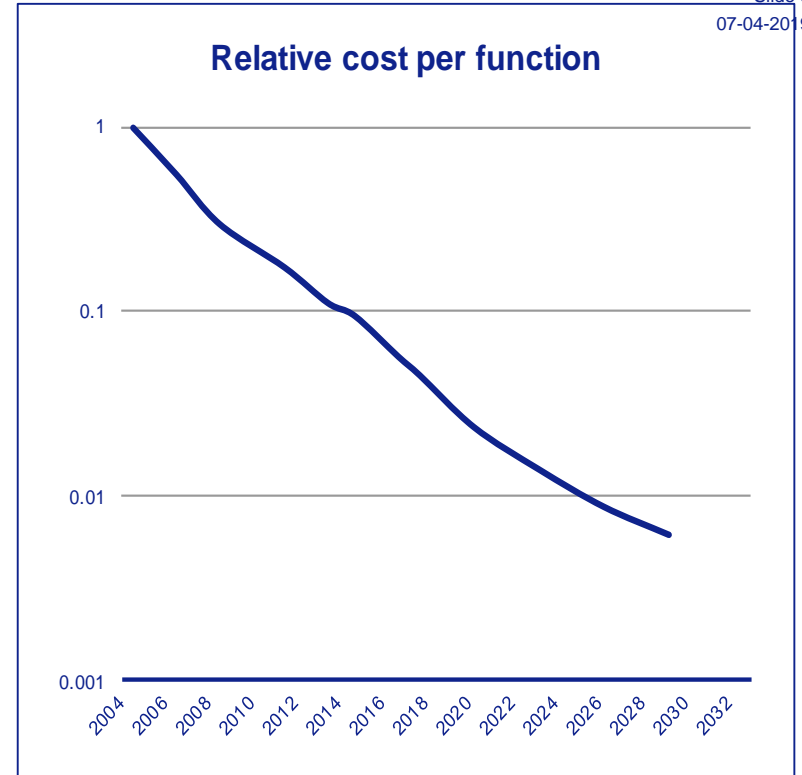
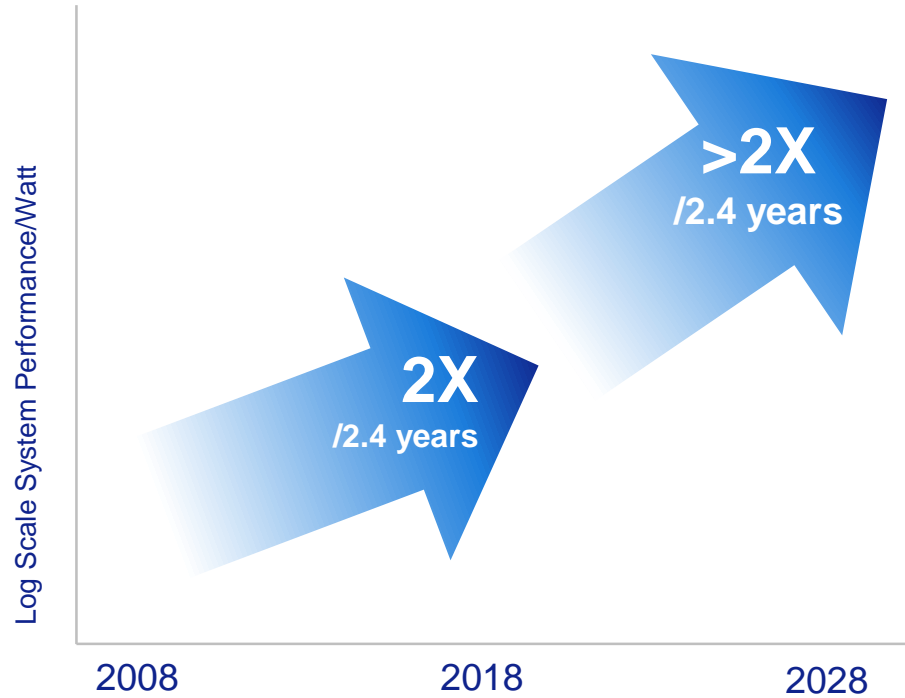
30M\$, 8 Mb, 5500 kg, 150 kW



2018

1000 \$, 512 MB + GB flash, 200 g, < 1W

The industry is driven by Moore's law, which continues, through ideas and value creation

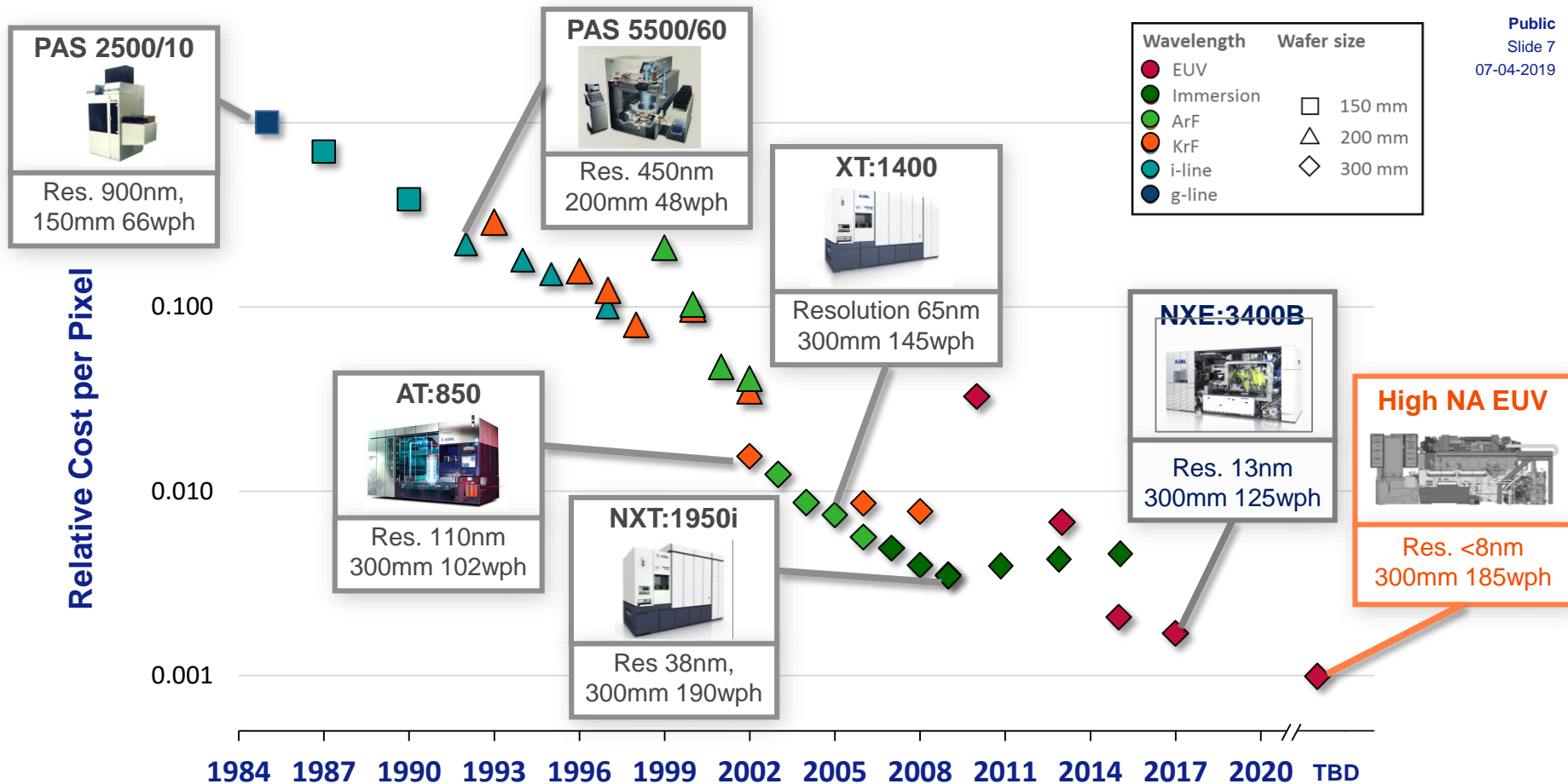


This is what we're doing it for!

¹Lisa Su, AMD, "Immersive era in consumer computing", IEDM, dec 2017

²Gordon Moore, "Progress in digital integrated Electronics" International; Electronic Device Meeting,, IEEE, 1975, p p 11-13

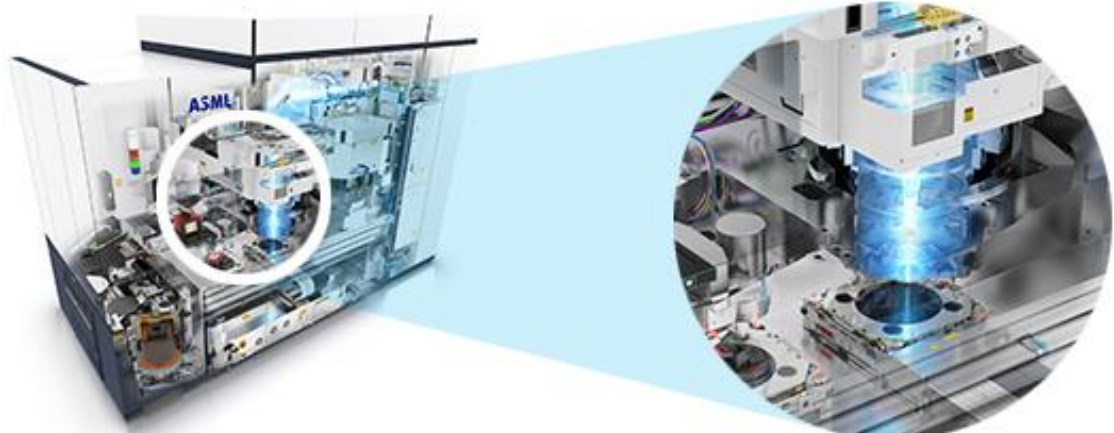
Our systems enable the faster, better, cheaper chips of tomorrow



ASML makes the machines for making IC's



Resolution:	>1 μ m	> 500 nm	> 400 to 90 nm	> 100 to 38 nm	> 32 to 16 nm
Overlay:	250 nm	100 nm	100 to 12 nm	20 to 4 nm	2 nm



Electronic Development within D&E ASML



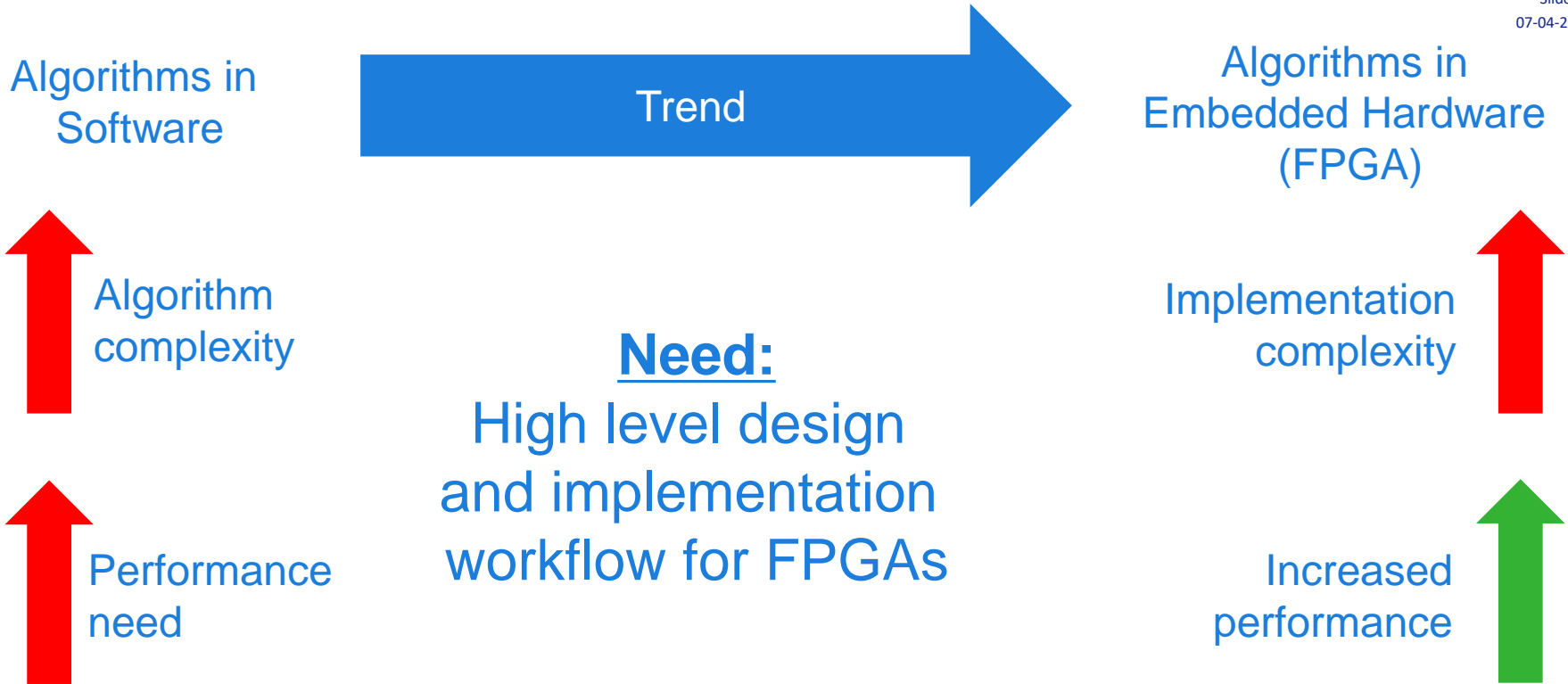
EDEV San Diego USA

EDEV Veldhoven The Netherland

EDEV Wilton USA

Goals and Challenges

Challenges



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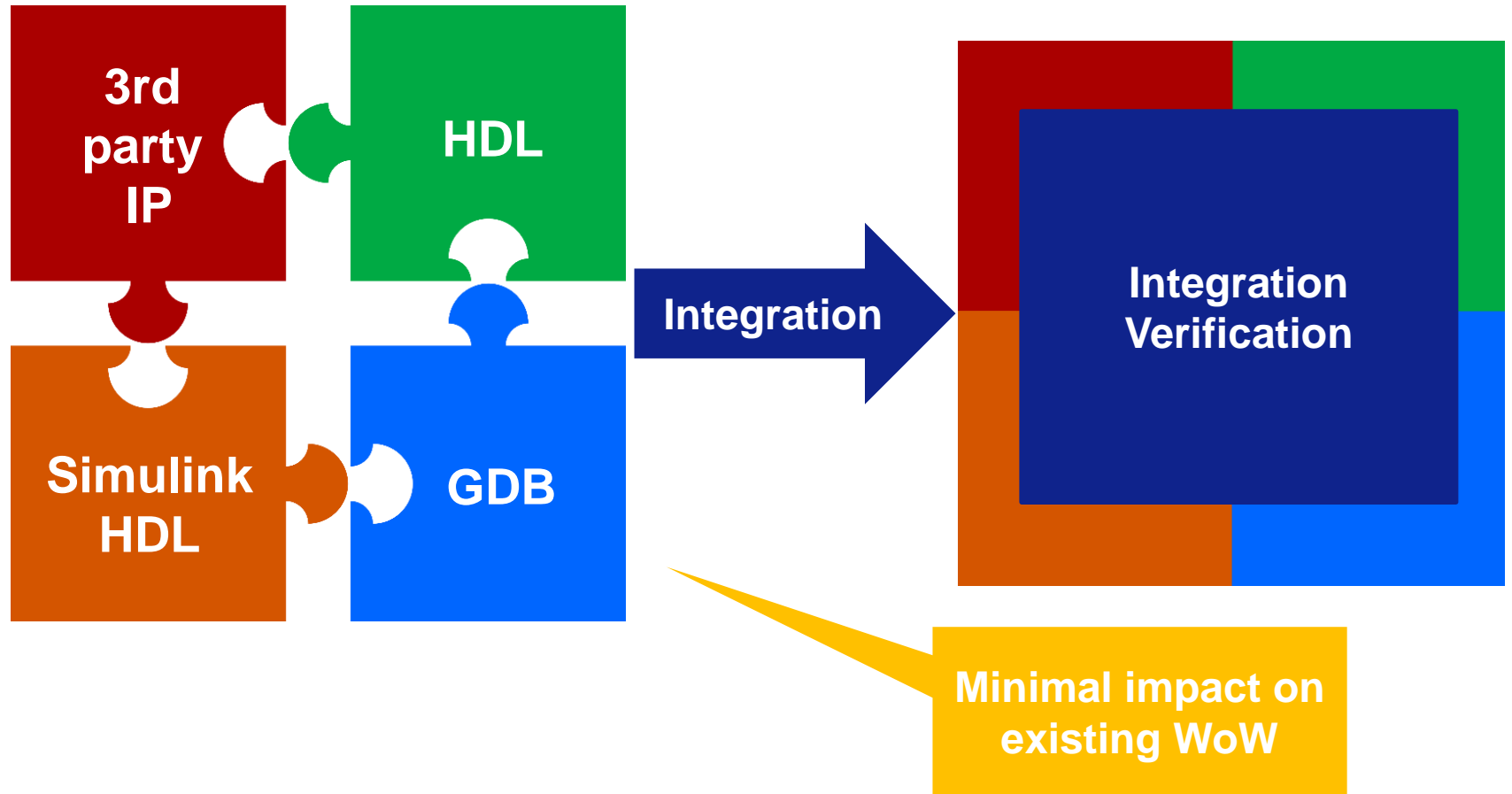
Goals

1. One ASML common method of developing algorithms in FPGAs
2. Make modeling, simulation and code generation accessible for ELF engineer
3. Reduce the gap between system architect and ELF engineer



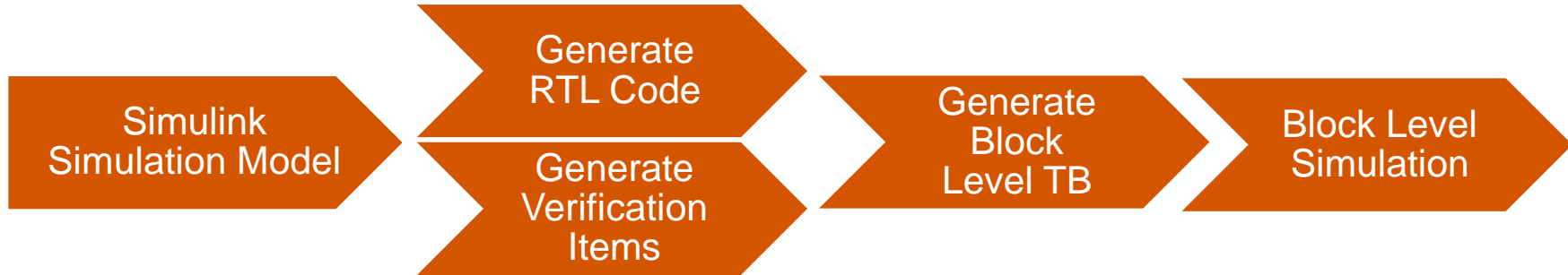
How we do it

ASML ELF Way-of-Working (WoW)



GDB = Generic Design Block, HDL = Hardware Description Language

ASML ELF Way-of-Working, elaborated



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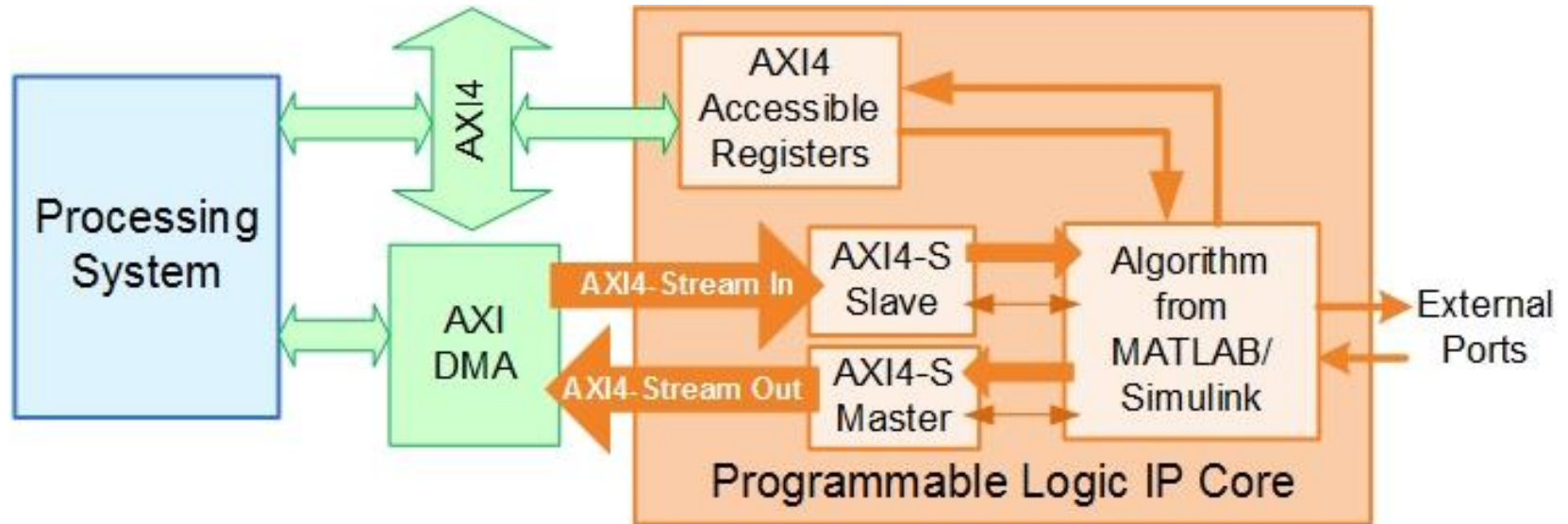
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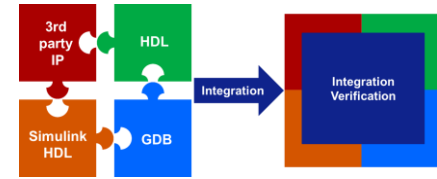
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ASML workflow to create algorithm subsystem, an example



Automated Build and Test



Public
Slide 18
11-03-2019



1. Buildfiles are used to automate the various tasks involved in the FPGA design flow
2. The “Build process” makes extensive use of (GNU) Make

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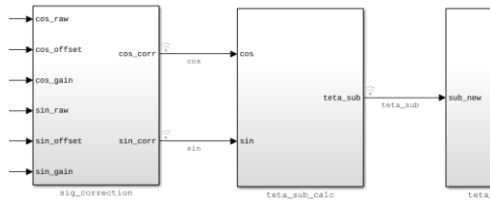
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Achievements and Outlook

Using HDL Coder in ELF projects

- **Established workflow within the entire ASML organization.**
 - IT team (IT4E) maintains development software and Linux servers for any ELF project
 - Standard use of HDL Code Generation in ELF Design Flow (DDM2/Buildfiles)
 - Integrated with workflow for communication protocols (GDB), integration tool (QSYS/Platform designer/Vivado Block design), hardware interfaces (VHDL)



```
Makefile for Matlab HDL Coder, Template version 20190125
Usage: make <target>

targets:
- all (default) : generate hdl
- hdl           : generate hdl
- generate      : generate hdl
- hdl_gui       : generate hdl with Matlab user interface enabled
- hdltb         : generate hdl testbench (validation of HDL against Matlab/Simulink results)
- hdltb_gui     : generate hdl testbench with Matlab user interface enabled
- simtb         : simulate generated validation testbench
- sim           : simulate design
- matlab/gui    : start matlab user interface
- edit          : start matlab user interface for editing Simulink design
- init          : create startup.m for default hdlcoder paths and setup
                  and setup cmd folder with template files
- clean         : removes all locally generated files
- distclean    : clean design dependencies recursively
- usage/help    : show available targets
jotol@ics106028149: /home/jotol/ddm/sbi_siab_Fw/matlab/lib_hdlcoder_rtp > █
```

- **Improved development of Digital Signal Processing (DSP) functions (vs. handwritten RTL and/or Testbench)**
 - Easier to make changes in a late stage of the project without compromising quality
 - Especially suited for complex DSP functions
- **Future work: automatic FPGA-In-the-Loop (FIL)**



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The image features the ASML logo in a bold, dark blue font on the left side. The background is a light blue gradient with several decorative elements: a large, semi-transparent blue arc in the upper left, and a series of thin, white, wavy lines that flow from the right side of the logo towards the right edge of the frame. The overall aesthetic is clean and modern.

ASML